INTEGRATED CIRCUIT HAVING MULTIPLE MEMORY TYPES AND METHOD OF FORMATION

Cross Reference to Related Applications

This application is related to the following copending U.S. Patent Applications:

(1) U.S. Serial No. 10/074,732 entitled "Method of Forming A Vertical Double Gate Semiconductor Device and Structure Thereof" assigned to the assignee hereof;

(2) U.S. Serial No. 10/443,375 entitled "Transistor With Independent Gate Structures" assigned to the assignee hereof; and

(3) U.S. Serial No. 10/443,908 entitled "Memory With Charge Storage Locations" assigned to the assignee hereof.

(4) U.S. Serial No. 10/427,141 entitled "Semiconductor Fabrication Process With Asymmetrical Conductive Spacers" assigned to the assignee hereof.

Field of the Invention

This invention relates to semiconductors, and more particularly to transistors for use in memories.

Reduced transistor structures have also brought about the ability to integrate both non-volatile (e.g. read-only-memory and Flash) and volatile (DRAM and SRAM) memory arrays for system on chip (SOC) applications. Typically different transistor structures implemented with differing processes are required to implement both non-volatile and volatile memory arrays. For example, a Flash memory transistor is implemented with a floating gate structure that is between a channel and a control gate. In contrast, a DRAM memory transistor is implemented with a planar transistor controlling a deep trench capacitor. The planar transistor uses a single plane channel that separates a source and a drain and that is controlled by an overlying gate. The requirement to implement both volatile and non-volatile memory arrays on a single integrated circuit therefore adds significant cost since differing processes and structures must be implemented. Additionally, due to the different transistor structures that are required, the operating characteristics of the transistors on a same integrated circuit may significantly differ.

Brief Description of the Drawings

The present invention is illustrated by way of example and not limited by the accompanying figures, in which like references indicate similar elements, and in which:

FIGs. 1-4 illustrate in cross-sectional form a field effect transistor in accordance with a first form of the present invention;

FIG. 5 illustrates in perspective form the field effect transistor of FIG. 4;

FIG. 6 illustrates in cross-sectional form the field effect transistor of FIG. 4 having electrical contacts;

sapphire. Overlying insulating layer 13 is a patterned fin semiconductor structure that forms a channel 14 of a FinFET (Fin Field Effect Transistor) that is silicon (either polysilicon, crystalline silicon, amorphous silicon, SiGe, germanium or a combination of any of these). Overlying the channel 14 is an oxide 16. Overlying the oxide 16 is a third gate 18 (the first and second gates to be identified below). In one form the third gate 18 is polysilicon. In another form, the third gate 18 may be a doped material using a conventional implant process. Overlying the third gate 18 is an oxide layer 20. In one form the oxide 20 is silicon dioxide. Overlying the oxide layer 20 is a nitride layer 22. In one form nitride layer 22 is silicon nitride. To form the illustrated structure of field effect transistor 10, each of channel 14, oxide 16, the third gate 18, oxide layer 20 and nitride layer 22 is formed by thermal growth of layers of the indicated material or deposition of the layers. The layers are conventionally patterned by etching the layers to create the structure of field effect transistor 10. Channel 14, oxide 16, the third gate 18 and nitride layer 22 have resulting exposed sidewalls.

Illustrated in FIG. 2 is further processing of field effect transistor 10 of FIG. 1. A conventional sacrificial oxide clean step is performed after the etching. Channel 14 has sidewalls that are illustrated in cross-sectional form in FIG. 2 as being opposing. An oxide layer 26 is formed on the sidewalls of channel 14 (first and second sidewalls in FIG. 2 that are on opposite sides of channel 14), and an oxide layer 28 is formed on the sidewall of the third gate 18. It should be understood that oxide layer 26 is actually a continuous layer of material around channel 14 and thus different reference numbers are not assigned to the left side and the right side. The oxide layer 26 and the oxide layer 28 may be either thermally grown or deposited in a conventional manner.